What is claimed is:

1. A method for manufacturing a ferroelectric random access memory (FeRAM) capacitor, the method comprising the steps of:

a) preparing an active matrix including a semiconductor substrate, a transistor, a bit line, a first interlayer dielectric (ILD), a second ILD and a storage node;

b) forming a first bottom electrode on the active matrix;

c) forming a third ILD on exposed surfaces of the first bottom electrode and the second ILD;

d) planarizing the third ILD till a top face of the first bottom electrode is exposed;

e) forming a second bottom electrode on a top face of the bottom electrode;

f) carrying out a first annealing process for deforming a surface of the second bottom electrode;

g) forming a dielectric layer on exposed surfaces of the first bottom electrodes, the second bottom electrode and the third ILD;

h) carrying out a second annealing process; and

i) forming a top electrode on the dielectric layer.

2. The method as recited in claim 1, wherein the step d) is carried out using a chemical mechanical polishing (CMP) technique.

3. The method as recited in claim 1, wherein the step d) is carried out using a blanket etch technique.

4. The method as recited in claim 1, wherein the step f) is carried out in an oxygen gas ambient for about an hour at a temperature in excess of about 400 ℃.

5. The method as recited in claim 4, after the step f), further comprising the step of carrying out a rapid thermal process (RTP) at a temperature ranging form about 400 ℃ to about 800 ℃.

6. The method as recited in claim 1, wherein the step h) is carried out in an oxygen gas ambient for about an hour at a temperature in excess of about 400 ℃.

7. The method as recited in claim 6, after the step h), further comprising the step of carrying out a rapid thermal process (RTP) at a temperature ranging form about 400 ℃ to about 800 ℃.

8. The method as recited in claim 1, wherein the first bottom electrode is a single layer employing a material selected from the group consisting of platinum (Pt), iridium (Ir), iridium oxide (IrO_x), ruthenium (Ru), rhenium (Re), rhodium (Rh), tungsten (W), titanium (Ti), titanium nitride

(TiN), titanium aluminum nitride (TiAlN), ruthenium oxide (RuO_2) and a combination thereof.

9. The method as recited in claim 1, wherein the second bottom electrode is a single layer employing a material selected from the group consisting of platinum (Pt), iridium (Ir), iridium oxide (IrO_X), ruthenium (Ru), rhenium (Re), rhodium (Rh), tungsten (W), titanium (Ti), titanium nitride (TiN), titanium aluminum nitride (TiAlN), ruthenium oxide (RuO_2) and a combination thereof.

10. The method as recited in claim 1, wherein the dielectric layer uses a ferroelectric material selected from the group consisting of strontium bismuth tantalate ($SrBi_2Ta_2O_9$, SBT), La-modified bismuth titanate ($(Bi,La)_4Ti_3O_{12}$, BLT) and lead zirconium titanate ($(Pb,Zr)TiO_3$, PZT).

11. The method as recited in claim 10, wherein the ferroelectric material has a perovskite crystal structure.

12. The method as recited in claim 10, wherein the ferroelectric material has a layered perovskite crystal structure.

13. The method as recited in claim 1, wherein the top electrode is a single layer employing a material selected from the group consisting of Pt, Ir, IrO_X, Ru, Re, Rh, W, Ti, RuO_2

and a combination thereof.

14. The method as recited in claim 1, wherein the top electrode is multi-layers employing a material selected from the group consisting of Pt, Ir, IrO_x, Ru, Re, Rh, W, Ti, RuO_2 and a combination thereof.